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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,808	06/22/2006	Rohini Krishnan	NL03 1474 US1	6873
65913	7590	02/27/2008	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			WHITE, DYLAN C	
			ART UNIT	PAPER NUMBER
			2819	
			NOTIFICATION DATE	DELIVERY MODE
			02/27/2008	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/583,808	<b>Applicant(s)</b> KRISHNAN ET AL.	
	<b>Examiner</b> DYLAN WHITE	<b>Art Unit</b> 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 07 November 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 June 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments filed 11/7/2007 have been fully considered but they are not persuasive.

Regarding Applicants argument, where Schultz concern is signal integrity and not power consumption of delay, does not matter regarding patentability. The Applicant having a different advantage does not preclude the prior art reference when it reads on the applicants claim language.

Regarding the Applicants argument where "Schultz has a single output" the Examiner respectfully traverses this assumption. Schultz discloses a single input/output (I/O) pad 202, this I/O pad can be connected to any number of elements or circuits through a transmission line. Having a single output pad does not prevent the pad from being connected to several transmitter or receiver circuit. Furthermore the number of circuits, one or more, connected to the I/O pad dictates the required fan-in/fan-out. This level of fan-in/fan-out is merely the overall load seen by the circuit in which the impedance is matched by the device to improve signal integrity, the higher the load for fan-out the more drive strength that is needed, and the lower the load the lower the drive strength needed.

The Examiner also respectfully traverses the argument regarding where the drive capability is not adjusted to meet a delay specification. The Schultz reference reduces the propagation delay (by reducing the ringing and noise through impedance matching)

to meet at least the required propagation delay between elements in the integrated circuit, therefor the drive capability is adjusted to meet a delay (propagation) specification.

### ***Claim Objections***

Claim 12 is objected to because of the following informalities: As stated in the previous Office Action, and repeated here; on line 3 "determining a load applied at at", the Examiner believes this should be applied to at. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 11 and 12, are rejected under 35 U.S.C. 102(b) as being anticipated by Schultz et al. (U.S. Pat. 6,445,245).

Regarding claim 1, Schultz discloses at least one circuit component (903) at which a load is applied (@ pad 943) that can vary during operation (col. 2, lines 37-40) where the configurable arrangement comprises: load determination means (1110, 1111, & 1101 within 963) for determining a load (connected to PAD 943) applied to the at least one configurable circuit component (903) having different fan-in or fan-out (load termination or drive strength) depending on a configuration (impedance matching circuit

@ Fig. 11; local DCI 963) of the circuit arrangement (impedance array 211 & 212) and responsive to the determination means (1110, 1111 & 1101) for adjusting drive capacity (in drive transistors arrays 211 & 212) of the at least one circuit component (buffer 903) to a value less than a maximum drive value (any value where not all transistors of the drive array P—P15 or N—N15 are turned on) meeting a delay specification (propagation delay of the signal between integrated circuit elements).

Regarding claim 2, Schultz discloses the determinations means (1110, 1111, & 1101 @ Fig. 11) is configured to determine the load based on configuration information (within configuration memory 1110, Fig 11; detailed drawing of DCI 963) to the circuit arrangement (Fig. 9).

Regarding claim 3, Schultz discloses where the configuration information is stored in a configuration memory (1110 @ Fig. 11).

Regarding claim 4, Schultz discloses where the configuration information comprises a configuration bit stream (col. 15, lines 29-30) defining at least one of an input load and output load (connected to PAD 903) of the at least one component (903).

Regarding claim 5, Schultz discloses where the adjusting means (1122 @ Fig. 11) is configured to vary a buffer (I/O buffer, via control signals FP/FN 1-7 & CP/CN 11-15) or a buffer number of the at least one component (903).

Regarding claim 6, Schultz discloses where the adjusting means (1122 @ Fig. 11) is configured to switch on or off buffers or buffer sections (transistors of Fig. 2) responsive to the determination means (1110, 1111, & 1101 @ Fig. 11).

Regarding claim 7, Schultz discloses where the adjusting means (1122 @ Fig. 11) is adapted to generate at least one control signal (any one of FP/FN 1-7 & CP/CN 11-15) for switching on or off buffer sections (transistor gate control @ Fig. 2).

Regarding claim 8, Schultz discloses where the adjusting means (1122 @ Fig. 11) is adapted to derive said control signal (one of FP/FN 1-7 & CP/CN 11-15) only from a most significant bit (col. 15, lines 29-33; MSB of four bit memory cell) of a selection signal obtained from the determination means (1110, 1111, & 1101).

Regarding claim 11, Schultz discloses where the circuit arrangement is a FPGA (col. 1, lines 13-16).

Regarding claim 12, Schultz discloses determining a load (connected to pad 943 @ Fig. 9) applied [to] at least one circuit component (903) having different fan-in or fan-out (load termination or drive strength) depending on a configuration impedance matching circuit @ Fig. 11; local DCI 963) of the configurable circuit; and adjusting the drive capacity (in drive transistors arrays 211 & 212) of the at least one circuit

component (903) responsive to the determination step (via 1110, 1111 & 1101) to a value less than a maximum drive capacity (any value where not all transistors of the drive array P—P15 or N—N15 are turned on) while still meeting a delay requirement (propagation delay of the signal between integrated circuit elements).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schultz et al. (U.S. Pat. 6,445,245) in view of Ajit (U.S. Pub. 2002/0113628).

Regarding claim 9, Schultz discloses that of claim 1 but fails to teach where the adjusting means is configured to vary the threshold voltage of a circuit elements in the arrangement.

Ajit teaches (Fig. 6) changing the transistor threshold voltage by biasing the transistor wells with biasing circuit (401), therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the output buffer disclosed by Schultz with the transistor biasing as taught by Ajit for varying the on/off voltage thresholds of the drive transistors.

Regarding claim 10, the combination discloses where the adjusting means (Ajit; 401 @ Fig. 10) is adapted to change at least one bias voltage (PMOS transistors) in response to the determination means (transistors 1001).

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art generally refers to impedance matching circuits.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DYLAN WHITE whose telephone number is (571)272-1406. The examiner can normally be reached on m-th 7:00- 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dylan White/  
Examiner, Art Unit 2819